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Convecs Team

**Formal modelling and verification methods of new
generations of networks of Programmable Logic
Controllers (PLC)**

Keywords: Compilation, Parallel Programming, Concurrent Systems, Formal Methods



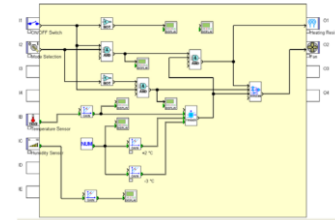
PLC devices

- Embedded systems
- Programmable via FBD (Functional Block Diagram)



Networks of PLCs

- High degree of asynchronous concurrency.
- Globally Asynchronous Locally Synchronous.
 - **Hard to design and debug**





Solution: CADP software toolbox

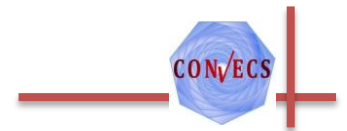
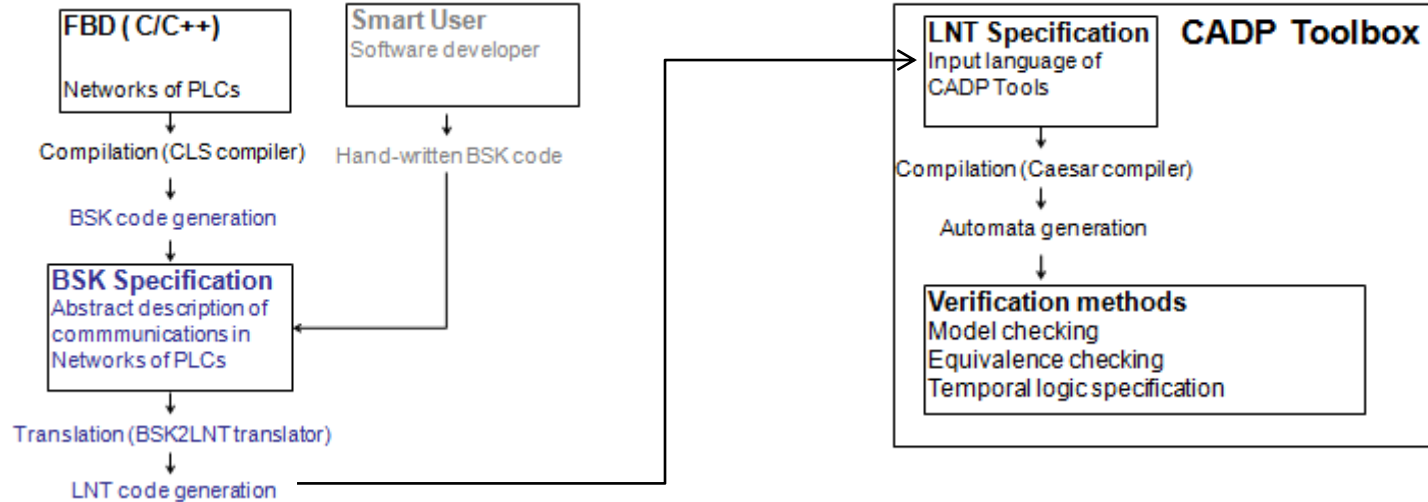
Formal methods for the design and verification of asynchronous concurrent systems

- Explicit-state verification
- Performance evaluation

<http://cadp.inria.fr/software>



Expected results





First Results (6 months)

- ❑ **Modelling individual PLCs**
BSK language formal definition (grammar and formal semantics)
- ❑ Translator of BSK programs into LNT language (BSK2LNT Tool)

